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JEDEC STANDARD No. 2

DIGITAL BIPOLAR PINOUTS FOR CHIP CARRIERS

JEDEC
Solid State Products Engineering Council

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DIGITAL BIPOLAR LOGIC PINOUTS

FOR CHIP CARRIERS

This JEDEC Standard was formulated under the cognizance of the JEDEC JC-40.1 Committee on BIPOLAR DIGITAL LOGIC INTEGRATED DEVICES.

Note: Numbering of JEDEC Standards follows a numerical sequence which does not necessarily relate to the publication date of the document.

PURPOSE AND SCOPE

Purpose

This Standard provides a chip carrier format for digital devices by defining pin functions and locations for 20, 28, 44, 52, and 68-terminal devices.

Scope

JEDEC Standard No. 2 should be of great value to both manufacturers and users of digital bipolar logic devices who need to be able to convert existing dual-in-line (DIP) package pin functions and locations to appropriate chip carrier package formats.

DIGITAL BIPOLAR LOGIC PIN-OUTS FOR CHIP CARRIERS

1. The standard chip carrier packages for Bipolar Digital Logic will be:

   A. Twenty (20) Terminals:

      For devices up to 20 external connections, the standard chip carrier package will be the .350 x .350 inch square format with 20 terminals on .050 inch centers.

   B. Twenty-eight (28) Terminals:

      For devices up to 28 external connections, the standard chip carrier package will be the .450 x .450 inch square format with 28 terminals on .050 inch centers.

   C. Forty-four (44) Terminals:

      For devices up to 44 external connections, the standard chip carrier package will be the .650 x .650 inch square format with 44 terminals on .050 inch centers.

   D. Fifty-two (52) Terminals:

      For devices up to 52 external connections, the standard chip carrier package will be the .750 x .750 inch square format with 52 terminals on .050 inch centers.

   E. Sixty-eight (68) Terminals:

      For devices up to 68 external connections, the standard chip carrier package will be the .950 x .950 inch square format with 68 terminals on .050 inch centers.

2. The pin-out definitions for Bipolar Digital Logic Integrated Circuits in the Dual-in-Line package configuration is universally accepted and documented in the industry's array of component catalogs. All pin-outs in chip carriers will be by reference to the de facto Dual-in-Line standards as follows:

   A. Twenty (20) Terminals:

      1. Devices requiring 14 connections in a 20 terminal chip carrier, see Figure 1.

      2. Devices requiring 16 connections in a 20 terminal chip carrier, see Figure 2.

      3. Devices requiring 20 connections in a 20 terminal chip carrier, see Figure 3.

   B. Twenty-eight (28) Terminals:

      1. Devices requiring 24 connections in a 28 terminal chip carrier, see Figure 4.

      2. Devices requiring 28 connections in a 28 terminal chip carrier, see Figure 5.

3. Bias Voltages for chip carriers will be designated by the following standard convention:

   The most positive bias voltage required by the device will be assigned to the highest numbered terminal. The most negative bias voltage required by the device will be assigned to the terminal number which is half the highest terminal number. Other required bias voltages will be assigned terminal numbers in accordance with the appropriate mapping figure, referenced under paragraph 2.

   When this convention conflicts with the mapping guidelines in paragraph 2 above, this convention will take precedence. The remaining connections then are assigned in sequence leaving the same "No connect" terminals as indicated in the figures referenced under paragraph 2.

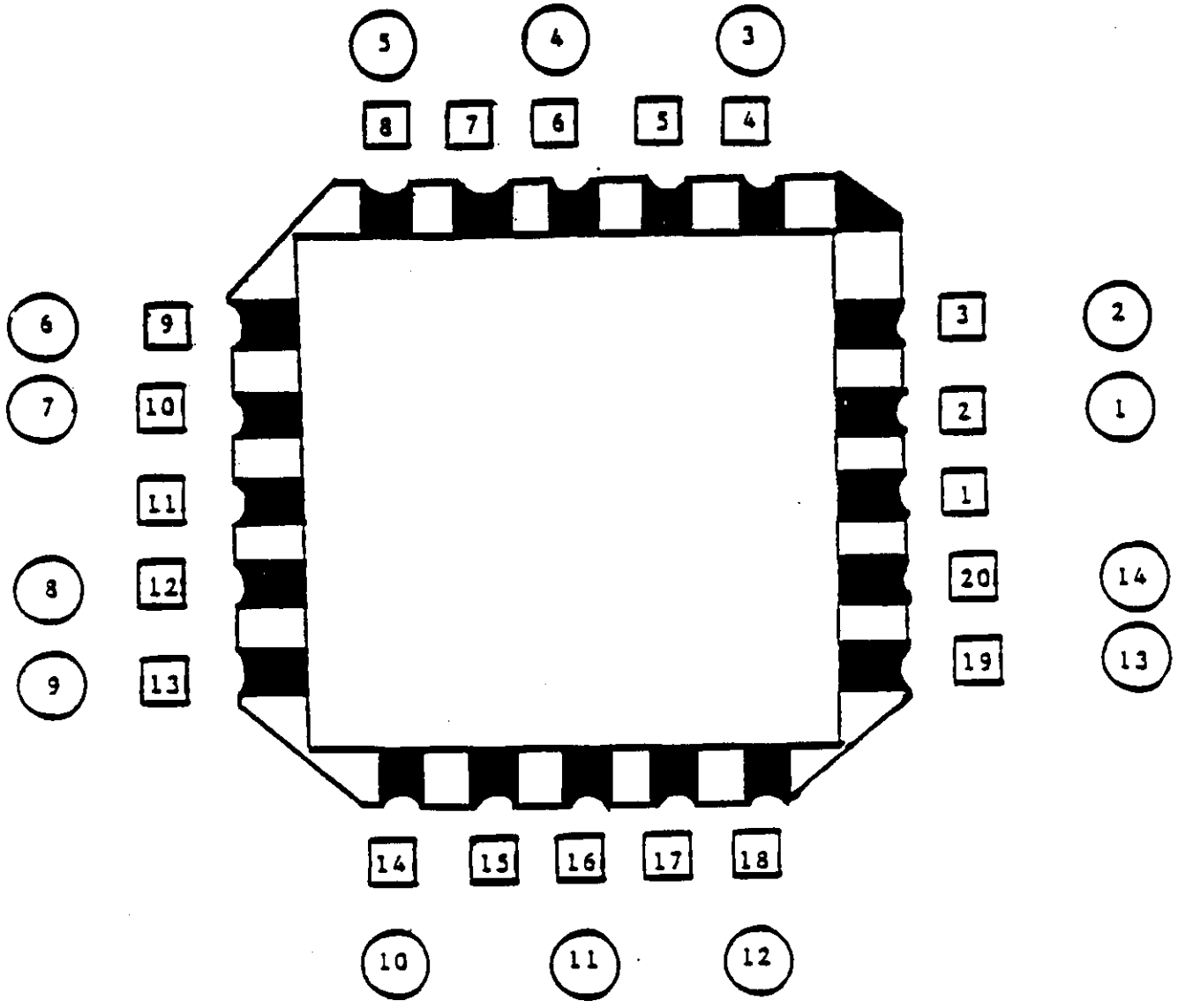
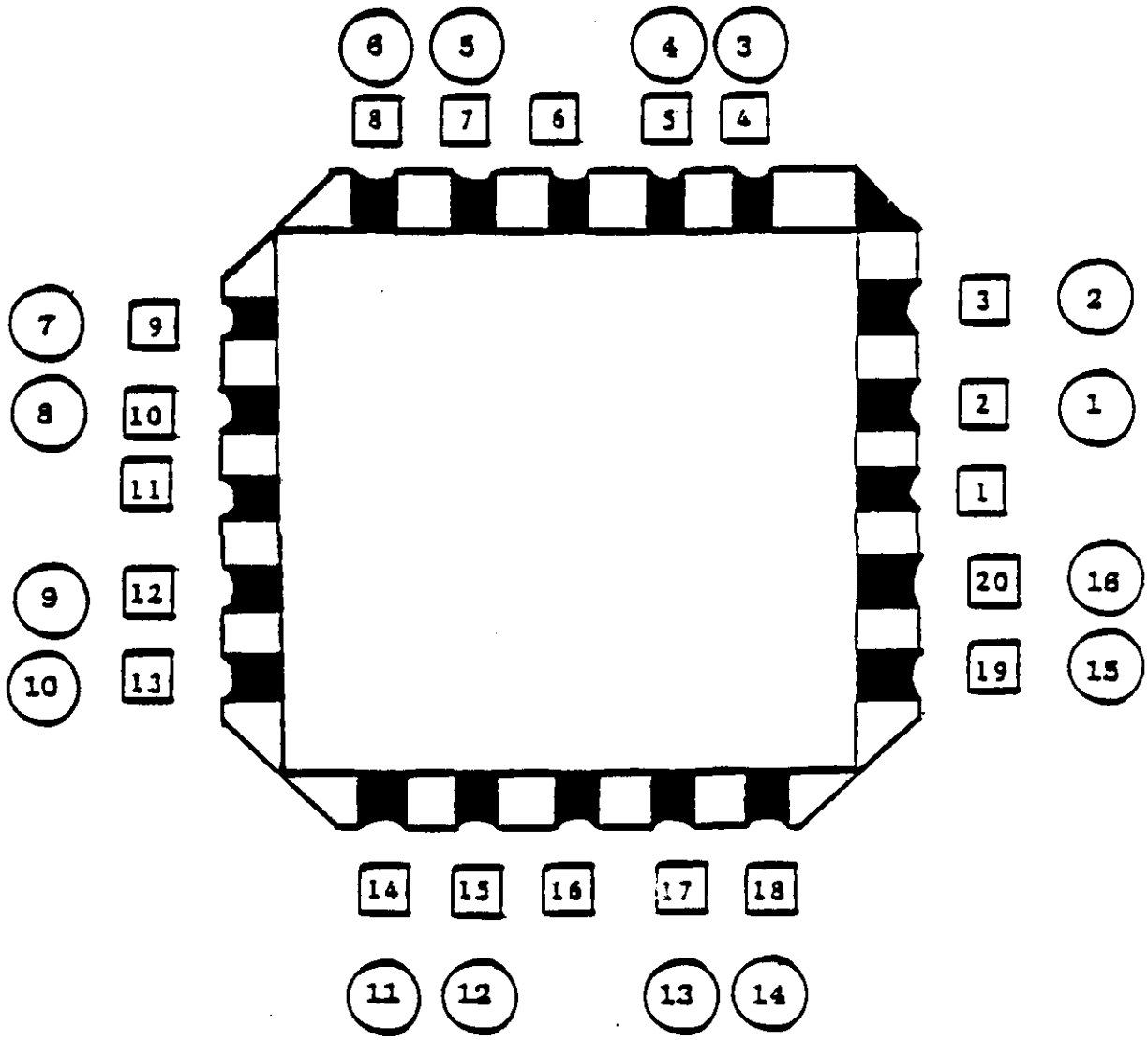


FIGURE 1: 14 - LEAD PIN-OUT FOR 20 TERMINAL CHIP CARRIER



(TOP VIEW)

□ CHIP CARRIER TERMINAL NUMBER

○ DUAL IN LINE LEAD NUMBER

FIGURE 2: 16 - LEAD PIN-OUT FOR 20 TERMINAL CHIP CARRIER

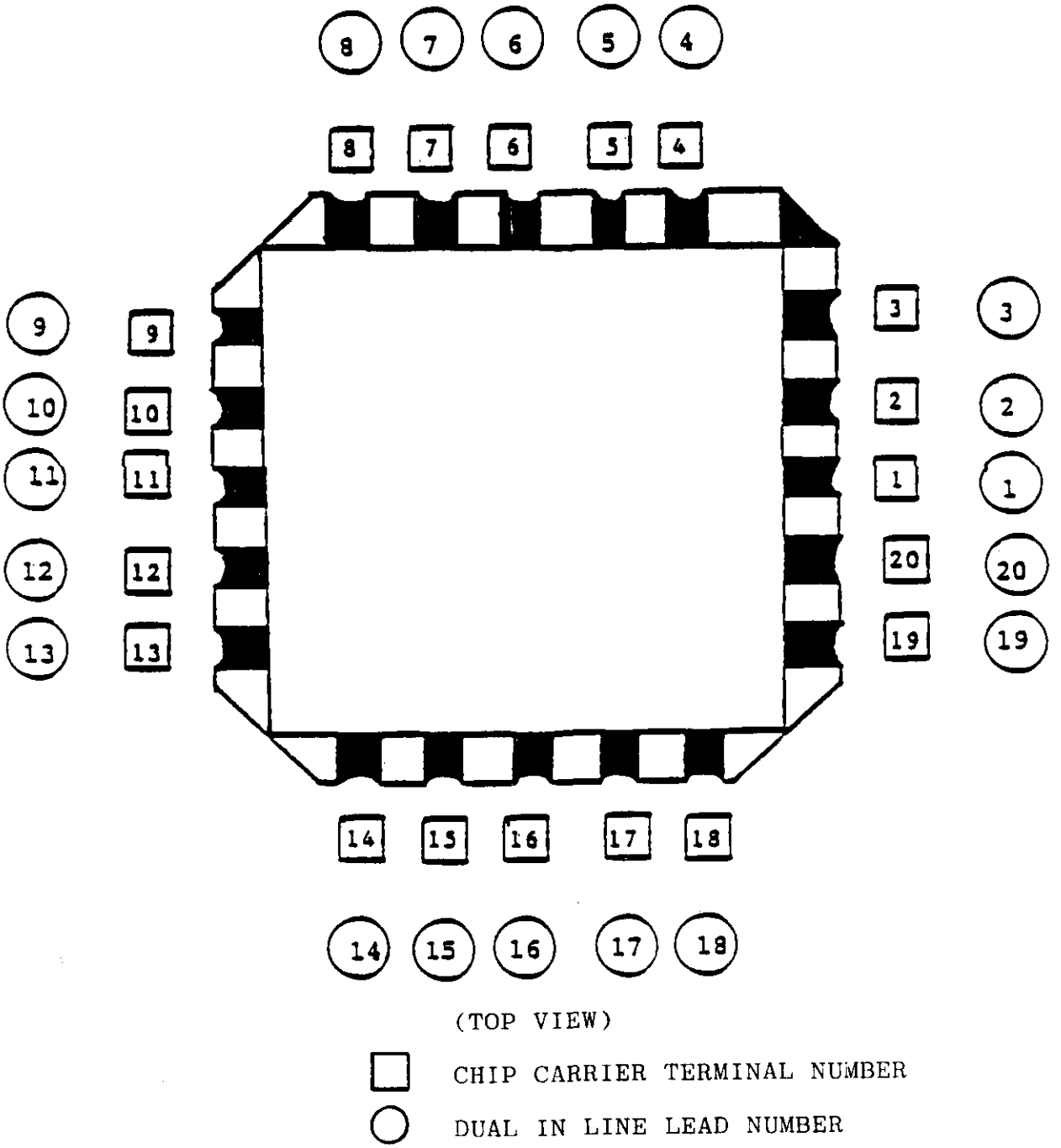


FIGURE 3: 20 - LEAD PIN-OUT FOR 20 TERMINAL CHIP CARRIER

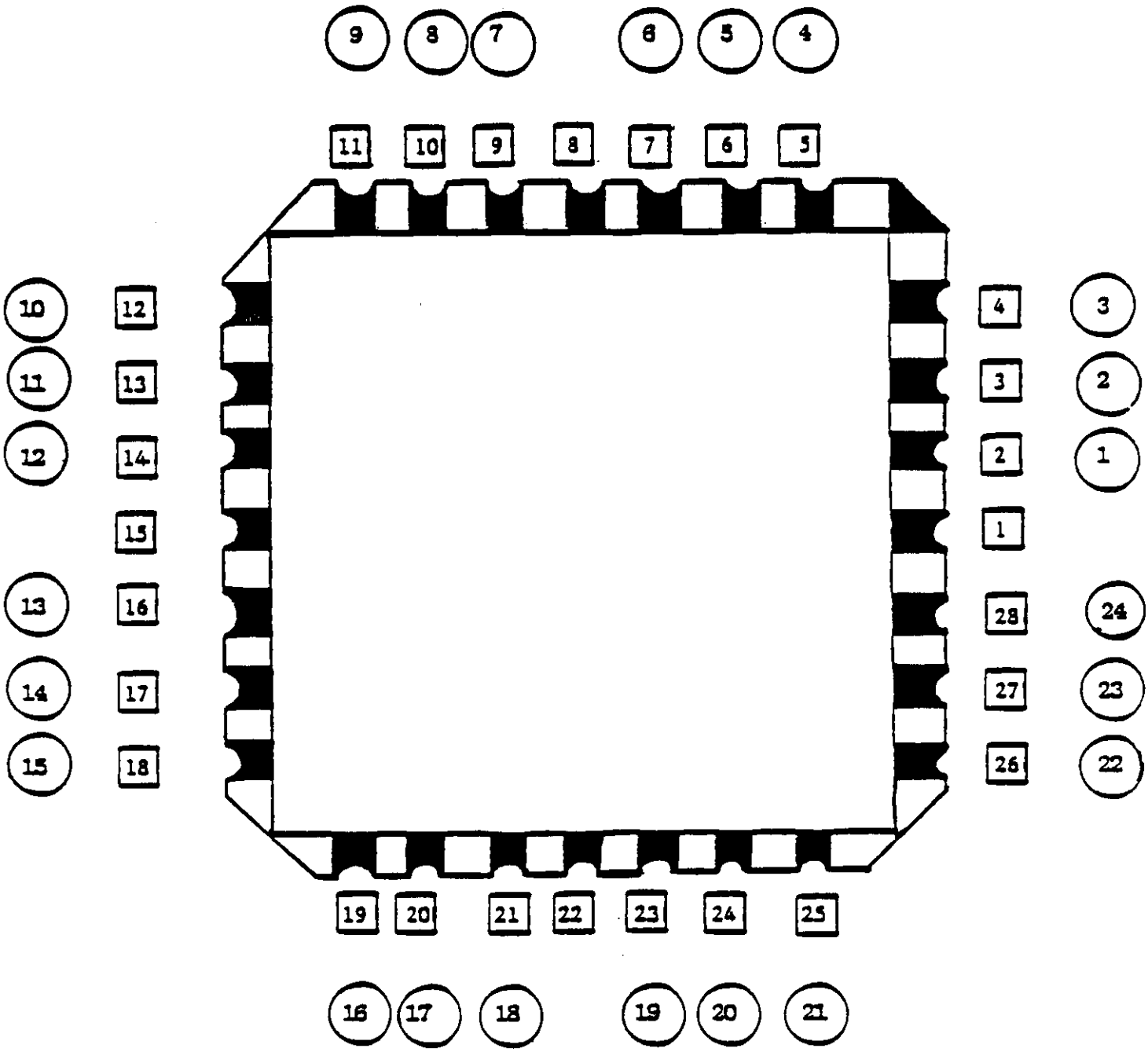


FIGURE 4: 24 - LEAD PIN-OUT FOR 28 TERMINAL CHIP CARRIER

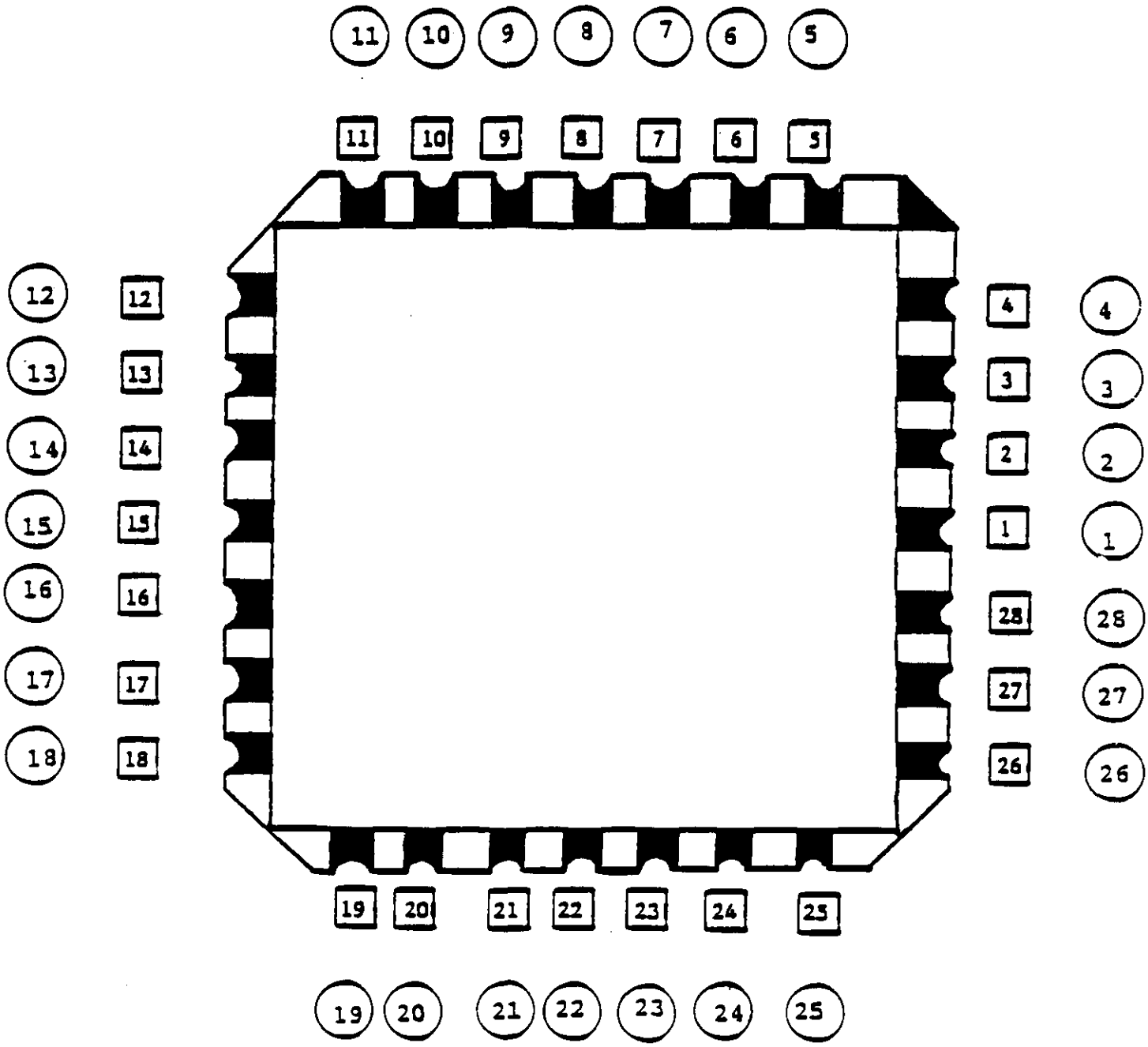


FIGURE 5: 28 - LEAD PIN-OUT FOR 28 TERMINAL CHIP CARRIER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